



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel Yellin et al. Art Unit: 2133

Serial No.: 09/880,707 Examiner: Joseph D. Torres Filed: June 12, 2001 Assignee: Intel Corporation

Title : LOW COMPLEXITY CHANNEL DECODERS

MAIL STOP AF

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicants submit this request under the New Pre-Appeal Conference Pilot Program described in the U.S. Patent and Trademark OG Notice, "New Pre-Appeal Brief Conference Pilot Program," dated 12 July 2005 and extended until further notice as of January 10, 2006. This request is being filed with a Notice of Appeal. Applicants request review of the matters discussed below by a panel of examiners, because the patentable subject matter rejections under 35 U.S.C. § 103(a) are clearly without basis.

Claims 1-22 and 29-31 are pending in the application. Of these, claims 1, 6, 9, 13, 16 and 19 are independent. Claims 1-6, 9-13, 16-19 and 22 are rejected under 35 U.S.C. § 103(a) as unpatentable over Kobayashi (U.S. Patent No. 6,029,264) in view of Steele et al. (U.S. Patent No. 4,393,276). Applicants have addressed these rejections in a reply to a final Office action and in an interview with the Examiner on August 10, 2006, but no agreement was reached and the rejections were maintained as final.

Accordingly, applicants ask that the panel review the Section 103(a) issue below, which Applicants submit will dispose of the entire appeal. Applicants reserve the right to expand these issues and/or present new issues when filing their appeal brief.

For the sake of brevity, this brief will focus on the method claims 1-5 (of which claim 1 is the only independent claim), although it should be understood that the positions applicants take in connection with the method claims apply with at least equal force to the other pending claims 6-22, and hence applicants request that these claims be considered by the panel as well.

CERTIFICATE OF MAILING BY EXPRESS MAIL
Express Mail Label No. EV 915265661 US
September 12, 2006
Date of Deposit

Applicant: Daniel Yellin et al. Attorney's Docket No.: 10559-449001 / P10766

Serial No.: 09/880,707

Attorney's Booket No.: 10333-4-3001711070
Assignee: Intel Corporation

Filed : June 12, 2001

Page : 2 of 4

Claim 1 of the present application recites

A method for decoding channel data comprising:
 receiving a packet of encoded data; and
 decoding the encoded packet using a look-up table that stores information
 approximating output of an algorithmic decoding process.

An example of decoding an encoded packet using a look-up table is disclosed on pages 5-6 of the present application in which a look-up table (LUT) 19 replaces SISO decoders 221A, 221B. Data packets encoded by encoder 120 are passed from demodulator 210 to the LUT 19 which includes table entries that correspond to an approximation of the output of a pre-specified conventional SISO decoder 221. As a result, the encoded data packets passed from demodulator 210 can be decoded using a look-up table rather than SISO decoders. Replacing the SISO decoders in this manner may reduce the processing power necessary for decoding encoded data packets.

The Final Action asserts that the ambiguity zone detector (AZD) of the Kobayashi patent corresponds to the claimed look-up table that decodes an "encoded packet" and also "stores information approximating output of an algorithmic decoding process" as recited in present claim 1.

Applicants respectfully disagree with respect to both allegations. The system disclosed in the Kobayashi patent neither decodes an "encoded packet using a look-up table" nor includes a look-up table that "stores information approximating output of an algorithmic decoding process." First, the Kobayashi patent does not disclose or suggest, in any way, decoding an encoded packet using the AZD. In contrast, the Kobayashi patent discloses that the AZD is a "threshold detector" which assigns erasure symbols to digits of a sequence that fall into ambiguous zones (column 6, lines 16-20). To be more precise, the AZD receives a sequence in which some or all of the received values of the sequence are ambiguous due to noise or interference (col. 8, lines 33-34). The AZD then assigns "generalized erasure" symbols to those ambiguous values (col. 8, lines 40-41) and subsequently outputs the *same* sequence that it received, with the exception of the ambiguous values having been replaced by the "generalized erasure" symbols (col. 8, lines

Applicant: Daniel Yellin et al.

Attorney's Docket No.: 10559-449001 / P10766

Serial No.: 09/880.707

Assignee: Intel Corporation

Serial No.: 09/880,707 Filed: June 12, 2001

Page : 3 of 4

34-45). An example of a relationship between values input to the AZD and the values that are output by the AZD is shown in FIG. 9b of the Kobayashi patent. The AZD of FIG. 9b merely assigns symbols "e" and "f" to input values that are located within specified ambiguous ranges "E" and "F." Neither the symbols "e" and "f" nor the sequence output by the AZD correspond to a data packet that has been decoded. Additionally, the Kobayashi patent does not disclose or suggest that replacing the ambiguous data values with symbols "e" and "f" provides any previously unknown information related either to the correct value of the decoded data or the correct value of the encoded data. Indeed, the Kobayashi patent even discloses that the output of the AZD is "fed to [a] decoder that attempts to resolve as many erasures/errors as possible" (col. 8, lines 66-67). Therefore, the Kobayashi patent clearly does not disclose "decoding an encoded packet using a look-up table" as recited in present claim 1.

Similarly, the Kobayashi patent does not disclose or suggest decoding, partially or otherwise, an encoded packet using the AZD in the concatenated decoding system of FIG. 11d, as asserted by the Final Office action. The concatenated decoding system shown in FIG. 11d includes an outer channel decoder $(D_3$ and $\pi_{23}^{-1})$ and a two-concatenated decoder D_{000} (ambiguous zone detector "AZD₂," error/erasure corrector "E/E correct", lower decoder D_2 , deinterleaver π_{12}^{-1} , upper decoder D_1 and interleaver π_{12} . Although the Kobayashi patent discloses that AZD₂ is included in decoder D_1 , the encoded data provided to D_1 is not decoded using AZD₂. In contrast, the data sequence entered into decoder D_1 de-interleaver π_{12}^{-1} , upper decoder D_1 and interleaver π_{12} (col. 8, line 66 – col. 11, line 17). The function of AZD₂ in decoder D_1 and interleaver π_{12}^{-1} (col. 8, line 66 – col. 11, line 17). The function of AZD₂ in decoder D_2 into a digital sequence that contains ambiguity signals (see col. 6, lines 17-20 and supra). It is apparent from the foregoing discussion that the Kobayashi patent clearly does not disclose or suggest "decoding an encoded data packet using a look-up table" as recited in claim 1 of the present application.

Furthermore, the AZD does not store "information approximating output of an algorithmic decoding process" as recited in present claim 1. The Final Office action asserts (page 4) that the output of AZD₂ is "off from the actual D_3 decoded and π_{23}^{-1} de-interleaved data by only the erasure values" and hence stores information approximating the output of an

Applicant: Daniel Yellin et al.

Serial No.: 09/880,707 Filed : June 12, 2001

Page

: 4 of 4

Attorney's Docket No.: 10559-449001 / P10766

Assignee: Intel Corporation

algorithmic decoding process. This is incorrect and misleading. Although the data sequence

received in the AZD may be provided from the output of a decoder, the Kobayashi patent does

not disclose or suggest that the AZD stores information approximating the output of an

algorithmic decoding process as recited in present claim 1. In contrast, the Kobayashi patent

discloses that values within a sequence received by the AZD may fall in "ambiguity zones E and

F" (col. 8, lines 38-39) when the noise induced by interference or a channel is large. As

discussed above, the AZD subsequently outputs erasure symbols e and f corresponding to the

ambiguity zones E and F. That is to say, the information output by the AZD is an approximation

of values within ambiguity zones E and F; it is not an approximation of the output of an

algorithmic decoding process.

For at least the foregoing reasons, the Kobayashi et al. patent neither discloses nor

suggests decoding an encoded packet using a look-up table that stores information approximating

output of an algorithmic decoding process, as is recited in claim 1. Nor does the Steele patent

disclose or suggest those features.

In view of the above, all of the claims should be in condition for allowance. A formal

notice of allowance is thus respectfully requested.

This request is filed with a Notice of Appeal. Please apply any other charges or credits to

deposit account 06-1050.

Respectfully submitted,

9/12/06

Level Dondal Samuel Borodach

Reg. No. 38,388

Fish & Richardson P.C. Attorneys for Intel Corporation 12390 El Camino Real San Diego, CA 92130

Telephone: (858) 678-5070

Facsimile: (858) 678-5099

30296819.doc